Remarks

Applicants herewith amend the specification to make reference to related U.S. patents and pending U.S. patent applications. Applicants respectfully request entry of these amendments.

DRAWING OBJECTIONS

In the non-final Office Action mailed October 18, 2004 (hereinafter "the Office Action"), the Examiner objected to the drawings under 37 C.F.R. § 1.83(a), stating that "the drawings must show every feature of the invention specified in the claims" and suggesting that the element "dielectric recess" is not shown. Applicants respectfully point out that a dielectric recess is, in fact, shown in the drawings, but Applicants have now highlighted the dielectric recess for clarity. Applicants direct the Examiner's attention to, for example, Figure 2, which shows metal bonding layers 106 interleaved with dielectric recesses to facilitate direct metal bonding between adjacent wafers 210 and 220. Thus, a "dielectric recess" is, in fact, shown and the figures are in compliance with 37 C.F.R. § 1.83(a).

For the sake of clarity, Applicant's have provided herewith an amended replacement sheet for Figure 2 which now includes numbered pointer 107 directed to some dielectric recesses. This pointer does not add new matter, since it merely indicates feature(s) which were present in the drawings as originally filed. Applicants have also presented herewith an amendment to the specification which adds a reference to "107" after the phrase "dielectric recess." This change is presented as a replacement paragraph. Applicants respectfully request entry of these amendments and withdrawal of the objections to the drawings.

CLAIM REJECTIONS UNDER 35 U.S.C. § 112

Also in the Office Action, the Examiner rejected Claim 3 under 35 U.S.C. § 112, first paragraph, asserting that "[t]he claim contains subject matter which was not described in the specification . . ." because the Examiner believed that a "dielectric recess" was not shown, and again asserting that "the feature is absent from the drawings." As noted above, a dielectric recess is, in fact, shown in the Figures. A dielectric recess can be seen in, for example, Figure 2, and, as noted above, Figure 2 has now been labeled with the number 107 and the specification amended to include a reference to the number 107 in discussing the dielectric recess. Thus, Applicants respectfully request that the rejection under 35 U.S.C. § 112 be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. § 102

Also in the Office Action, the Examiner rejected Claims 1, 7, 9, 14, 16, and 21 under 35 U.S.C. § 102(e) as being anticipated by Hikita, et al., U.S. Patent number 6,724,084 (hereinafter "Hikita"). By rejecting these claims under 102(e) the Examiner asserts that Hikita teaches each and every element of the rejected claims. However, such is not the case. Applicants respectfully assert that the Examiner has mischaracterized the claims and that the rejection under 102(e) was improper.

Applicants first note that each of the rejected claims contain the limitation "wafer" and / or "wafers." Hikita, in contrast, is directed to "semiconductor chips" and does not teach processes directed to wafers. Hikita clearly distinguishes between semiconductor chips and wafers, and teaches processes directed to chips, not wafers. Thus, Hikita fails to anticipate Applicants' claims directed to wafers.

For example, Hikita teaches that "semiconductor substrate 22 in a wafer form is cut into chips by means of a dicing saw" (Hikita, column 15, line 54). Thus, Hikita teaches that chips and

wafers are not the same thing. Therefore, the Examiner is incorrect in stating that "Hikita discloses a wafer bonding method" (Office Action, page 3, paragraph 5). In fact, Hikita discloses methods directed to chips, not to wafers, and thus does not anticipate Applicants' claim elements that are directed to wafers.

As another example, the Examiner states that Hikita teaches "a first wafer" and "a second wafer," as required by Claim 1 (Office Action, page 3, paragraph 5). The Examiner points to "'bottom' 80 in figures 4a, 4b" and "'top' wafer in figures 4a, 4b" in support of the rejection, but in fact these portions of Hikita do not disclose wafers, they disclose chips. This is clearly stated in the Hikita specification, which discusses figures 4a and 4b by stating "FIGS. 4A and 4B are diagrams for explaining how semiconductor chips 80 . . . are stacked . . ." (Hikita, column 10, lines 66-67).

The Examiner has failed to show that Applicants' claims 1, 7, 9, 16, or 21 are anticipated by Hikita because Hikita does not teach wafers. Hikita teaches chips. As the Examiner stated, the prior art "does not suggest applying a barrier to an outer edge of a bonded *wafer*. . ." (Office Action, page 5, paragraph 9, emphasis added). Therefore, the Examiner has failed to set forth a *prima facie* rejection under section 102 because Hikita does not teach each and every element of the rejected claims. Applicants traverse these rejections and respectfully request that they be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103

Also in the Office Action, the Examiner rejected Claims 2, 10, 17, and 18 under 35 U.S.C. § 103(a) as being unpatentable over Hikita in view of Chooi, et al., U.S. Patent number 6,340,608 (hereinafter "Chooi"). The Examiner relies on Hikita to teach all the claim elements except for bond pads made of copper, relying on the combination with Chooi to teach the copper limitation. However, as noted above, Hikita fails to teach any of the claim limitations directed to "wafers"

because Hikita teaches chips. Furthermore, the Examiner does not rely on Chooi to teach the missing "wafers" limitations.

Thus, since the combination of Hikita and Chooi fails to teach each and every element of the rejected claims, the Examiner has failed to set forth a *prima facie* case of obviousness under section 103(a). Furthermore, Applicants respectfully assert that the Examiner has mischaracterized Chooi and that there is no motivation to combine Chooi with Hikita because Chooi teaches away from Hikita.

The Examiner asserts that Chooi teaches copper bond pads, and asserts that Chooi teaches copper interconnection pads are advantageous (Office Action, page 5, top half of page). However, Chooi teaches something else entirely, namely the use of a photosensitive resin for forming interconnections as *an improvement over copper interconnect termination pads*. Chooi states "a key step of the invention" leaves a "photosensitive resin plug 32' *over copper metal bump 26*" (Chooi, column 3, lines 15-18, emphasis added). That is, Chooi teaches that it is preferable *not to use* copper bonding, but to use a photosensitive resin instead. Thus, as the specification in Chooi makes clear, Chooi is directed to bonding via photosensitive resin.

Indeed, where the Examiner called on column 1, lines 5-18 of Chooi to support the combination of Chooi and Hikita (Office Action, page 5, top half of page), the cited language actually teaches that copper bond pads are disadvantageous. Lines 5-18 state that "[t]he present invention overcomes these limitations" of copper interconnect termination pads, which is the opposite of what the Examiner asserts. Chooi in fact teaches that the use of copper interconnect pads is an inferior approach. Therefore, one skilled in the art would not be motivated to combine Chooi with Hikita to develop a wafer bonding method.

Thus, Applicants respectfully assert that the combination of Chooi with Hikita was improper, and, further, the proposed combination of Chooi with Hikita fails to teach all the elements of the

rejected claims. Applicants traverse these rejections and respectfully request that they be withdrawn.

Conclusion

In the Office Action, the Examiner indicated that claims 4-6, 8, 11-13, 15, 19, 20, and 22 are drawn to allowable subject matter. Applicants agree, and further assert that the remaining claims are likewise drawn to allowable subject matter. Applicants respectfully traverse the claim rejections and request that all the pending claims be allowed to issue. If the Examiner has any questions, Examiner is invited to contact the undersigned at (703) 633-0927. If any fee insufficiency or overpayment is found, please charge the insufficiency or credit the overpayment to Deposit Account 02-2666.

Respectfully submitted,

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